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REPLY UNDER 37 C.F.R. § 1.116
EXPEDITED PROCEDURE
EXAMINING GROUP 2115

PATENT
5500-68500/TT4418

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/061,671
Filed: February 1, 2002
Inventor:
Michael A. Filippo

Title: Apparatus and Method for Selective Clock Control to Reduce Power Consumption in an Integrated Circuit

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Examiner: Wang, Albert C.
Group/Art Unit: 2115
Atty. Dkt. No: 5500-68500

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Robert C. Kowert
Name of Registered Representative

Signature

July 11, 2005
Date

RESPONSE TO FINAL ACTION OF MAY 17, 2005

Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

This paper is submitted in response to the Final Action of May 17, 2005, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.